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L23: Entry 1 of 1 File: USPT Jul 2, 2002

DOCUMENT-IDENTIFIER: US 6414670 B1
TITLE: Gate driving circuit in liquid crystal display

Abstract Text (1):
A gate driving circuit in a liquid crystal display is disclosed which can minimize a power consumption by avoiding unnecessary drive of gate line drivers. The gate driving circuit is used in a liquid crystal display having a liquid crystal panel with thin film transistors and pixel electrodes for displaying an image, a source driving circuit for applying video data to a source line in the liquid crystal panel, and a gate driving circuit for applying a driving signal to a gate line in the thin film transistors. The gate driving circuit includes a plurality of gate line drivers connected in series for applying the driving signal to the gate line, and a plurality of clock generation controlling units corresponding to the plurality of gate line drivers each for controlling a timing of a clock signal to a respective gate line driver, thereby controlling a driving timing of the respective gate line driver.

Brief Summary Text (6):
Referring to FIG. 1a, a liquid crystal display is, in general, provided with a liquid crystal panel 11, a driver unit 12 having a plurality of gate line drivers (GD) around the liquid crystal panel 11, and a source line driver unit 13 having a plurality of source line drivers (SD). As shown in FIG. 1b, the liquid crystal panel 11 is provided with a plurality of gate lines G1, G2, G3, - - - , Gn, a plurality of source lines S1, S2, S3, - - - , Sn in a direction crossing each of the gate lines, a thin film transistor 11a formed at a crossing point of the gate lines and the source lines, and a liquid crystal capacitor 11b connected to its respective thin film transistor 11a.

Brief Summary Text (12):
FIG. 3 illustrates the operation waveform diagram of the gate line driver. Referring to FIG. 3, the STV1 signal is provided at a first falling edge of the CPV signal (clock signal), shifted to the second shift register SR2 through the first shift register SR1, and passed through the first level shifter LS1 and the buffer BF1, to provide a high level out1 signal to be applied to the first gate line at a second rising edge of the CPV signal. Then, the signal shifted to the second shift register SR2 at the next falling edge of the CPV signal is shifted to the third shift register SR3, passed through the second level shifter LS2 and the second buffer BF2, and provides a high level out2 signal to the second gate line at a third rising edge of the CPV signal. Thus, out1 to out 154 signals are provided in sequence matched to the rising edges of the clock signal clk according to the foregoing method. After providing the signals out1 up to out154, the STV2, an operation signal for the next gate line driver, is provided. The STV2 signal, being equivalent of the STV1 signal for the next gate line driver, provides 154 signals in sequence as explained before.

Brief Summary Text (14):
With reference to the waveforms shown in FIG. 5, if one of the plurality of gate lines in the liquid crystal panel 11 is selected (i.e., a high signal is applied), other gate lines are applied with low signals. A driving signal (i.e., the high signal) applied to one of the gate lines is shifted in succession synchronous to every rising edge of the clock signal. Of the signals provided from the first gate

line driver 41-1 in FIG. 4, when the signal out154 is provided, the STV2 signal is provided synchronized to the falling edge of the clock signal. The STV2, equivalent of the STV1 for the second gate line driver 41-2, causes the second gate line driver 41-2 to provide signals from out1 to out154 in succession. When all the gate line drivers complete all operation in succession, one image is displayed on the liquid crystal panel.

Brief Summary Text (18):
An object of the present invention is to provide a gate driving circuit in a liquid crystal display with minimized power consumption by eliminating the unnecessary drivings of gate line drivers.

Brief Summary Text (20):
To achieve these and other advantages and in accordance with the purpose of the present invention, as embodied and broadly described, the gate driving circuit of the present invention is to be used in a liquid crystal display having a liquid crystal panel with thin film transistors and pixel electrodes for displaying an image, a source driving circuit for applying a video data to a source line in the liquid crystal panel, and a gate driving circuit for applying a driving signal to a gate line in the thin film transistor. The gate driving circuit includes a plurality of gate line drivers connected in series for applying the driving signal to the gate line, and clock generation controlling units provided to correspond to the gate line drivers for controlling a timing of the clock signal to respective gate line drivers to control a driving timing of respective gate line drivers.

Drawing Description Text (6):
FIG. 2 illustrates a conventional gate line driver in a liquid crystal display;

Drawing Description Text (7):
FIG. 3 illustrates operation waveforms of the conventional gate line driver in a liquid crystal display;

Detailed Description Text (4):
The operation of the clock generation controlling unit will be explained referring to FIG. 6. Acting as a reset signal for the first and second flipflops 61a and 61b, a signal from the first AND gate 61d is at a low level initially. The first flipflop 61a, provided with an STV1 signal as a clock signal, is of a positive edge trigger to be triggered at a rising edge of the STV1 signal to provide a high level signal. However, since the STV2 signal which acts as a clock signal for the second flipflop 61b is still at a low level, a signal from the second flipflop 61b is at a low state. The low level signal from the second flipflop 61b is changed to a high level as it passes through the inverter 61c and provided to the first AND gate 61d, together with the high level signal from the first flipflop 61a. Accordingly, the first AND gate 61d provides a high level signal.

Detailed Description Text (5):
The second AND gate 61e subjects a signal from the first AND gate 61d and the clock signal clk to AND operation. The second flipflop 61b is of a negative edge trigger, to be triggered at a falling edge of the STV2 signal to provide a high level signal. Therefore, since the signal from the first AND gate is turned to a low level while the signal from the first AND gate 61d is at a low level, the first flipflop 61a and the second flipflop 61b, receiving the STV1 and the STV2 as clock signals respectively, are reset.

Detailed Description Text (6):
FIG. 7 illustrates an operation timing diagram of the clock generation controlling unit shown in FIG. 6. Referring to FIG. 7, the clock signal clk1, a CPV signal to the gate line driver (not shown), is provided only between a rising edge of the STV1 signal and a falling edge of the STV2 signal. Therefore, signals out1.about.out154, each triggered at a rising edge of the clk1 signal in succession, are provided to the gate line in succession. Once the STV1 signal is provided, the driving signals out1.about.out154 are provided, and the STV2 signal is provided at a falling edge of the 154.sup.th signal. As shown in FIG. 7, a level of the X point shown in FIG. 6 is kept high from generation of the STV1 signal to generation of the STV2 signal. Accordingly, the second AND gate 61e receives a signal from the first AND gate 61d

and the clock signal clk, and provide the clock signal clk to the gate line driver as it is.

Detailed Description Text (8):
Referring to FIG. 8, the gate driving circuit includes a plurality of gate line drivers 81-1, 81-2, 81-3, - - - , 81-n connected in series for operating in succession in response to the driving signal STV and the clock signal. The gate driving circuit also includes a plurality of clock generation controlling units 82-1, 82-2, 82-3, - - - , 82-n each adapted to control the clock signal to respective gate line driver for selective application thereto. The clock generation controlling units 82-1, 82-2, 82-3, - - - , 82-n are maintained at an enable state only when the gate line drivers 81-1, 81-2, 81-3, - - - , 81-n connected thereto is in operation, and are maintained at a disable state when the gate line drivers 81-1, 81-2, 81-3, - - - , 81-n not connected thereto is in operation. Thus, the clock signal provided to each of the gate line drivers 81-1, 81-2, 81-3, - - - , 81-n is controlled individually, and the clock signal is not applied to the gate line drivers which should not be driven.

Detailed Description Text (12):
The clock signal clk1 used as a CPV signal to the first gate line driver 81-1 is provided only between a rising edge of the STV1 signal and a falling edge of the STV2 signal. Accordingly, triggered at a rising edge of the clk1 signal, signals out1.about.out154 are provided to the gate lines in succession. As the second gate line driver 81-2 receives the STV2 signal of the first gate line driver 81-1 as its equivalent STV1 signal, the second gate line driver 81-2 receives the clock signal clk2 between a rising edge of the signal and a falling edge of the STV2 signal of the second gate line driver 81-2. Accordingly, the signals out1.about.out154 provided from the second gate line driver 81-2 are triggered at rising edges of the clk2 signal and apply driving signals to respective gate lines.

CLAIMS:

1. A gate driving circuit in a liquid crystal display having a liquid crystal panel with thin film transistors and pixel electrodes for displaying an image, a source driving circuit for applying video data to a source line in the liquid crystal panel, and a gate driving circuit for applying a driving signal to a gate line in the thin film transistors, the gate driving circuit comprising:

a plurality of gate line drivers connected in series for applying the driving signal to the gate line; and

a plurality of clock generation controlling units corresponding to the plurality of gate line drivers each for controlling a timing of a clock signal to a respective gate line driver and each including a first flip flop connected as a toggle flip flop, thereby controlling a driving timing of the respective gate line driver.

3. The gate driving circuit as claimed in claim 1, wherein each of the plurality of clock generation controlling unit includes:

the first flipflop being operative triggered at a rising edge of the clock signal;

a second flipflop being operative triggered at a falling edge of the clock signal;

an inverter for inverting an output of the second flipflop;

a first logic device for subjecting an output of the inverter and an output of the first flipflop to a logical operation; and

a second logic device for subjecting an output of the first logic device and an external clock signal to a logical operation.

8. The gate driving circuit as claimed in claim 5, wherein each of the plurality of clock generation controlling units includes:

the first flipflop being operative triggered at a rising edge of the clock signal;

a second flipflop being operative triggered at a falling edge of the clock signal;

an inverter for inverting an output of the second flipflop;

a first logic device for subjecting an output of the inverter and an output of the first flipflop to a logical operation; and

a second logic device for subjecting an output of the first logic device and an external clock signal to a logical operation.

12. The gate driving circuit as claimed in claim 11, wherein the respective gate line driver is triggered at a rising edge of the output signal from the second logic device to provide a driving signal to the gate lines in succession, and provides the second control signal to be used as a clock signal for the second flipflop once a last driving signal is provided.

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**Search Results -**

| Terms | Documents |
|---|---|
| display with data electrodes and light with emit$ with layer and scan$ with electrodes | 98647 |

**Database:** US Patents Full-Text Database
US Pre-Grant Publication Full-Text Database
JPO Abstracts Database
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IBM Technical Disclosure Bulletins

**Search:** L4 and row with driv$3 with circuit and column with driv$3 with circuit

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## Search History

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| Set Name side by side | Query | Hit Count | Set Name result set |
|---|---|---|---|
| | *DB=USPT; PLUR=YES; OP=OR* | | |
| L4 | display with data electrodes and light with emit$ with layer and scan$ with electrodes | 98647 | L4 |
| L3 | L1 and LEDs | 0 | L3 |
| L2 | L1 and light with emitting with element | 0 | L2 |
| L1 | 5754160 | 8 | L1 |

END OF SEARCH HISTORY

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**Search Results -**

| Terms | Documents |
|---|---|
| L4 and row with driv$3 with circuit and column with driv$3 with circuit | 874 |

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**Search:** L5

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## Search History

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| Set Name side by side | Query | Hit Count | Set Name result set |
|---|---|---|---|
| *DB=USPT; PLUR=YES; OP=OR* | | | |
| L5 | L4 and row with driv$3 with circuit and column with driv$3 with circuit | 874 | L5 |
| L4 | display with data electrodes and light with emit$ with layer and scan$ with electrodes | 98647 | L4 |
| L3 | L1 and LEDs | 0 | L3 |
| L2 | L1 and light with emitting with element | 0 | L2 |
| L1 | 5754160 | 8 | L1 |

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**Search Results -**

| Terms | Documents |
|---|---|
| L22 and column with driving with circuit | 7 |

**Database:**
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- EPO Abstracts Database
- Derwent World Patents Index
- IBM Technical Disclosure Bulletins

**Search:** L23 and control$3 with current with data with electrodes

Refine Search | Recall Text | Clear

**Search History**

**DATE: Sunday, October 20, 2002** Printable Copy Create Case

| Set Name side by side | Query | Hit Count | Set Name result set |
|---|---|---|---|
| | *DB=USPT; PLUR=YES; OP=OR* | | |
| L23 | L22 and column with driving with circuit | 7 | L23 |
| L22 | L21 and row with driving with circuit | 8 | L22 |
| L21 | Image with display and data with electrodes and light with emit$3 with layer | 228 | L21 |
| L20 | L18 and emit$3 | 1 | L20 |
| L19 | L18 and light with emitting | 0 | L19 |
| L18 | 5032832 | 6 | L18 |
| L17 | L14 and LEDs | 3 | L17 |
| L16 | L14 and light with emitting with element | 0 | L16 |
| L15 | L14 and light emitting with element | 23510 | L15 |
| L14 | 4935670 | 10 | L14 |
| L13 | L10 and control$3 with current | 1 | L13 |
| L12 | L10 and function with control$3 with current | 0 | L12 |
| L11 | L10 and function with control$3 with current with data with electrodes | 0 | L11 |
| L10 | L4 and column with driving with circuit | 14 | L10 |
| L9 | L4 and column with driving with circuit with function with control$3 current | 810265 | L9 |
| L8 | L4 and column with driving with circuit with function with control$3 current | 810265 | L8 |
| L7 | L4 and column with driving with circuit with function with control$ current | 810265 | L7 |
| L6 | L5 and control$ with current with data with electrodes | 0 | L6 |
| L5 | L4 and column with driving with circuit | 14 | L5 |
| L4 | L3 and two with region | 168 | L4 |
| L3 | ((345/$3).ccls.) and display and data with electrodes and light emit$ and scanning with light and "row driving circuit" | 1458 | L3 |
| L2 | ((345/74 )!.CCLS. ) and display and data with electrodes and light emit$ and scanning with light and "row driving circuit" | 2 | L2 |
| L1 | 5754160 | 8 | L1 |

END OF SEARCH HISTORY

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L64: Entry 3 of 5 File: USPT Apr 6, 1999

DOCUMENT-IDENTIFIER: US 5892504 A
TITLE: Matrix display device and its method of operation

Abstract Text (1):
A matrix display device comprising a row and column array of display elements (14), e.g. LC display elements, each of which is connected in series with a two terminal non-linear device (15), such as a MIM, between associated row and column address conductors (16,17) and drive means (20,22,25) for applying drive voltages to the picture elements comprising a scanning signal circuit (20) and a data signal circuit (22) for applying selection signals and data signals respectively to the sets of address conductors, in which a sensing circuit (40) provides a control signal (V.sub.1) indicative of current flowing in one, or more, address conductor (16) of one set during the application of selection signals to that conductor which determines the drive voltages applied to the picture elements, preferably by adjustment of the selection signal level, so as to compensate for changes over time in the threshold characteristics of the non-linear devices. Four or five level scanning signal drive schemes may be used. Such compensation may be effected periodically or continually in operation of the display device.

Brief Summary Text (2):
This invention relates to a matrix display device comprising sets of row and column address conductors, a row and column array of picture elements operable to produce a display, each of which comprises an electro-optic display element connected in series with a two terminal non-linear device exhibiting a threshold characteristic between a row conductor and a column conductor, and picture element drive means connected to the sets of address conductors for applying drive voltages to the picture elements comprising a scanning signal drive circuit for applying selection signals to the conductors of one set and a data signal drive circuit for applying data signals to the conductors of the other set. The invention relates also to a method of operating such a display device.

Brief Summary Text (4):
For acceptable quality of display it is important that the non-linear devices of the matrix array demonstrate substantially similar threshold and I-V characteristics in operation so that the same drive voltages applied to any picture element in the array produce substantially identical visual results, for example in the case of a liquid crystal display device, as regards picture element transmission levels. Differences in the threshold or turn-on point of the non-linear devices can appear directly across the electro-optical material producing different display effects from picture elements addressed with the same drive voltages.

Brief Summary Text (9):
According to one aspect of the present invention a matrix display device as described in the opening paragraph is characterised in that the drive means includes a sensing circuit which is arranged to provide a control signal indicative of electrical current flowing in at least one address conductor of the one set during the application of selection signals to that address conductor, and a voltage control circuit to which the control signal is supplied for providing an output determining the drive voltages applied by the drive means to the picture elements in accordance with the value of the control signal.

Brief Summary Text (10):
According to another aspect of the present invention, a method of operating a matrix

display device of the kind described in the opening paragraph is characterised by the steps of deriving a control signal indicative of the electrical current flowing in at least one address conductor of the one set during the application of selection signals to that address conductor and controlling the drive voltages applied by the drive means to the picture elements in accordance with the value of the control signal.

Drawing Description Text (2):
A matrix display device, comprising a liquid crystal display device, and its method of operation, in accordance with the present invention will now be described, by way of example, with reference to the accompanying drawing figures, in which:

Detailed Description Text (3):
Referring to FIG. 1, the display device is intended to display video information, for example TV pictures, and comprises an active matrix addressed liquid crystal display panel 10 consisting of m rows (1 to m) with n picture elements (1 to n) in each row. Each picture element 12 consists of a twisted nematic liquid crystal display element 14 connected electrically in series with a bidirectional non-linear resistance device 15 exhibiting a threshold characteristic and acting as a switching element between a row conductor 16 and a column conductor 17. The picture elements 12 are addressed via sets of row and column conductors 16 and 17 which are in the form of electrically conductive lines carried on respective opposing faces of two, spaced, glass supporting plates (not shown) also carrying the opposing electrodes of the liquid crystal display elements. The devices 15 are provided on the same plate as the set of row conductors.

Detailed Description Text (5):
Active matrix liquid crystal display devices employing two terminal non-linear resistance elements as switching elements in series with the display elements are generally well known and hence the foregoing description of the main features and general operation of the display device with regard to FIG. 1 has deliberately been kept brief for simplicity. For further information reference is invited to the aforementioned publications describing such types of display devices. The row and column driver circuits 20 and 22 are of conventional form, as described for example in GB-A-2129182, and are controlled by a timing and control circuit, generally referenced at 25, which comprises a video processing unit 30, a timing signal generation unit 31 and a power supply unit 32. The row drive circuit 20 comprises a digital shift circuit and switching circuit to which timing signals and voltages determining the scanning signal waveforms are applied from the circuit 25 through supply lines 26 and 27. The column driver circuit 22 comprises one or more shift register/sample and hold circuits and is supplied with video data signals along line 28 from the video processing unit 30 and derived from a video (TV signal containing picture and timing information. Timing signals are supplied to the circuit 22 along the line 29 in synchronism with row scanning to provide serial to parallel conversion appropriate to the row at a time addressing of the panel 10.

Detailed Description Text (8):
In known active matrix LC display devices using two terminal non-linear devices such as diodes or MIMs as the active elements, changes in the operating characteristics of the devices can produce changes in the display performance. If there is a change in the current through, and hence the voltage drop across, the non-linear device during the selection period when the device is conducting to charge the display element then there is a consequential change in the voltage appearing across the display element. The nature of this change depends on the drive scheme employed. In the case of a display device driven with a four level row drive scanning signal waveform, then a change in the threshold voltage level, i.e. the "on" level, of a non-linear device causes a change in the amplitude of the display element voltage and hence its transmission. FIG. 2(a) illustrates a typical scanning signal waveform, V.sub.R, according to this drive scheme. This consists of a selection signal portion of magnitude Vs.sup.1 and of duration corresponding to a row selection period which is followed immediately by a hold signal portion of lower voltage, V.sub.H.sup.1 but of like polarity for the remainder of the field period. These signal portions are inverted in successive fields so that in the next field the row conductor concerned is addressed with a selection signal V.sub.S.sup.2 followed by a hold signal V.sub.H.sup.2. FIG. 2b illustrates the voltage across a

display element, V.sub.LC, for a picture element whose non-linear device's threshold level changes, the solid and dotted lines representing the display element voltage in the case of respectively comparatively low and comparatively high threshold levels.

Detailed Description Text (29):
Although in the above described embodiments, the non-linear devices comprise bidirectional devices, it should be understood that the invention is applicable also to matrix display devices, and their method of operation, of the kind in which non-linear devices comprising unidirectional devices are used, for example as described in EP-A-0299546, whose disclosure is incorporated herein by reference, in which each display element is connected in series with a unidirectional diode element between respective row and column address conductors and also in series with a second unidirectional diode element to a respective reference voltage conductor which is common to the display elements in the same column, and in which a five level scanning signal waveform is applied to the row conductors.

Detailed Description Text (31):
From reading the present disclosure, various modifications will be apparent to persons skilled in the art. Such modifications may involve other features which are already known in the field of active matrix display devices and which may be used instead of or in addition to features already described herein.

CLAIMS:

1. A matrix display device comprising sets of row and column address conductors, a row and column array of picture elements operable to produce a display, each of which comprises an electro-optic display element connected in series with a two terminal non-linear device exhibiting a threshold characteristic between a row conductor and a column conductor, and picture element drive means connected to the sets of address conductors for applying drive voltages to the picture elements comprising a scanning signal drive circuit for applying selection signals to the conductors of one set and a data signal drive circuit for applying data signals to the conductors of the other set, characterised in that the drive means includes a sensing circuit which is arranged to provide a control signal indicative of electrical current flowing in at least one address conductor of the one set in response to the application of selection signals to that address conductor, and a voltage control circuit to which the control signal is supplied for determining the drive voltages applied by the drive means to the picture elements in accordance with the value of the control signal.

2. A matrix display device according to claim 1, characterised in that the voltage control circuit provides an output which determines the level of the selection signals in accordance with the control signal.

3. A matrix display device according to claim 2, characterised in that the level of the selection signals is adjusted in accordance with the difference between the control signal and a reference level.

4. A matrix display device according to claim 2, characterised in that the scanning signal drive circuit applies a scanning signal waveform which comprises reset signals in addition to the selection signals and in that the output of the voltage control circuit also determines the level of the reset signals.

5. A matrix display device according to claim 2, characterised in that the scanning signal circuit is electrically connected to a supply line to which a potential determining the level of the selection signal is supplied and in that the sensing circuit is arranged to sense electrical current flowing in that supply line.

6. A matrix display device according to claim 1, characterised in that the sensing circuit provides a voltage signal which varies in accordance with electrical current sensed thereby and in that the control signal is obtained by correcting the voltage signal in accordance with the level of data signals applied to address conductors of the other set.

7. A matrix display device according to claim 6, characterised in that the control signal is obtained from a subtractor circuit to which the voltage signal from the sensing circuit and a data signal supplied to the data signal drive circuit are applied.

8. A matrix display device according to claim 7, characterised in that said signals are applied to the substractor circuit respectively via matched low pass filters.

9. A matrix display device according to claim 1, characterised in that the sensing circuit is arranged to provide said control signal at selected periods and in that the data signal drive circuit is operable to supply a predetermined potential level to the address conductors of the other set during said periods.

10. A matrix display device according to claim 9, characterised in that the control signal is indicative of electrical current in an address conductor associated with a row of picture elements to which a predetermined data signal is applied each time a selection signal is applied to that address conductor.

11. A matrix display device according to claim 1, characterised in that the non-linear devices comprise MIMs.

12. A matrix display device according to claim 1, characterised in that the electro-optic display element of each picture element comprises a liquid crystal display element.

13. A method of operating a matrix display device comprising sets of row and column address conductors, a row and column array of picture elements operable to produce a display, each of which comprises an electro-optic display element connected in series with a two terminal non-linear device exhibiting a threshold characteristic between a row conductor and a column conductor, and picture element drive means connected to the sets of address conductors for applying drive voltages to the picture elements comprising a scanning signal drive circuit for applying selection signals to the conductors of one set and a data signal drive circuit for applying data signals to the conductors of the other set, characterised by the steps of deriving a control signal indicative of the electrical current flowing in at least one address conductor of the one set in response to the application of selection signals to that address conductor and controlling the level of the drive voltages applied to the picture elements in accordance with the value of the control signal.

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| Terms | Documents |
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**Database:** US Patents Full-Text Database
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**Search:** L36

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## Search History

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| Set Name side by side | Query | Hit Count | Set Name result set |
|---|---|---|---|
| | *DB=USPT; PLUR=YES; OP=OR* | | |
| L36 | L35 and row with driv$ with circuit | 3 | L36 |
| L35 | Alexander same eisen | 62 | L35 |
| L34 | L33 and current with data with electrodes | 0 | L34 |
| L33 | L32 and row with driv$3 with circuit | 9 | L33 |
| L32 | Ali same zamani | 65 | L32 |
| L31 | L28 and control$ with current with data with electrodes | 0 | L31 |
| L30 | L28 and column with driv$3 with circuit | 0 | L30 |
| L29 | L28 and column with driv$3 with circuit and control$3 with current with data with electrode | 0 | L29 |
| L28 | display with row with driv$with circuit and simultaneous$3 with scan$ with electrodes and lighting with horizontal | 2 | L28 |
| L27 | display with row with driv$3 with circuit and simultaneous$ with driv$ with scan$3 with electrodes and light$3 | 16 | L27 |

| | | | |
|---|---|---|---|
| L26 | Image with display and data with electrodes and light with emit$3 with layer | 228 | L26 |
| L25 | L23 and control$3 with current with data with electrodes | 0 | L25 |
| L24 | L23 and current with density | 1 | L24 |
| L23 | L22 and column with driving with circuit | 7 | L23 |
| L22 | L21 and row with driving with circuit | 8 | L22 |
| L21 | Image with display and data with electrodes and light with emit$3 with layer | 228 | L21 |
| L20 | L18 and emit$3 | 1 | L20 |
| L19 | L18 and light with emitting | 0 | L19 |
| L18 | 5032832 | 6 | L18 |
| L17 | L14 and LEDs | 3 | L17 |
| L16 | L14 and light with emitting with element | 0 | L16 |
| L15 | L14 and light emitting with element | 23510 | L15 |
| L14 | 4935670 | 10 | L14 |
| L13 | L10 and control$3 with current | 1 | L13 |
| L12 | L10 and function with control$3 with current | 0 | L12 |
| L11 | L10 and function with control$3 with current with data with electrodes | 0 | L11 |
| L10 | L4 and column with driving with circuit | 14 | L10 |
| L9 | L4 and column with driving with circuit with function with control$3 current | 810265 | L9 |
| L8 | L4 and column with driving with circuit with function with control$3 current | 810265 | L8 |
| L7 | L4 and column with driving with circuit with function with control$ current | 810265 | L7 |
| L6 | L5 and control$ with current with data with electrodes | 0 | L6 |
| L5 | L4 and column with driving with circuit | 14 | L5 |
| L4 | L3 and two with region | 168 | L4 |
| L3 | ((345/$3).ccls.) and display and data with electrodes and light emit$ and scanning with light and "row driving circuit" | 1458 | L3 |
| L2 | ((345/74 )!.CCLS. ) and display and data with electrodes and light emit$ and scanning with light and "row driving circuit" | 2 | L2 |
| L1 | 5754160 | 8 | L1 |

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